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THE GEORGE WASHINGTON UNIVERSITY
SCHOOL OF ENGINEERING
AND APPLIED SCIENCE
WASHINGTON, D.C. 20052

Continuing Engineering Education

PRESENTS

Course No. 574

INTEGRATED CIRCUIT ENGINEERING

June 8-12, 1981

Course No. 696

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June 15-17, 1981

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June 22-25, 1981

Course No. 828

COMPUTER COMMUNICATIONS CONCEPTS

June 29-30, 1981

Course No. 796

DIGITAL INTEGRATED CIRCUITS

July 13-17, 1981

(202) 676-6106
(800) 424-9773
TELEX 64374 (International)

Course No. 574

INTEGRATED CIRCUIT ENGINEERING

June 8-12, 1981

COURSE OBJECTIVES

This intensive course will examine all aspects of integrated circuit engineering. Presentations have been arranged to provide the participants with a comprehensive understanding of the design, fabrication, and testing of integrated circuits.

WHO SHOULD ATTEND

Engineers, scientists, managers, and others working in the electronics industry who want to increase their knowledge of integrated circuits.

DESCRIPTION

To facilitate the participants' understanding of circuit design and layout, a discussion of bipolar circuit design and layout will be undertaken at the beginning of the program. This discussion will follow a step-by-step procedure according to certain ground rules and minimum spacing criteria. The design and layout of n-MOS circuits will be discussed.

The course will cover many different fabrication techniques, including the introduction of impurities by means of epitaxy, diffusion and ion implantation, oxidation and nitridation of silicon for masking and passivation purposes, and metalization by means of evaporation and sputtering.

The final portion of the course will address in-process measurement and testing of integrated circuits, and assembly and packaging techniques.

PREREQUISITE

Although there is no formal prerequisite for this course, some knowledge of solid state electronics would be helpful.

OUTLINE

First Day

Physics and Chemistry of Processing
- Evaporation
- Sputtering
- Epitaxial growth
- Diffusion
- Ion implantation
- Oxidation of silicon
- Deposition of silicon nitride
- Cleaning of silicon wafers
- Properties of impurities in silicon
- Photoresists

Second Day
- Junction-isolated bipolar circuits
- Beam-lead technology
- Countersunk oxide isolation
- V-groove isolation
- Dielectric isolation
- Inverted chips
- Collector-diffusion isolation
- Thick-oxide metal-gate MOSFET circuits
- Self-aligned polysilicon gate n-MOS process
- CMOS
- Application of ion implantation to SIC processing

Third Day

Design of Silicon Integrated Circuits
- Introduction
- Pattern generation
- Mask-alignment tolerance
- Minimum layout spacings
- Minimum-area transistor
- Layout of silicon integrated circuits
- Computer aids for integrated circuit layout (CAD)
- n-MOS LSI and VLSI

Fourth Day A.M.

Thin-Film Circuits
- Introduction
- Conduction in metal films
- Substrates
- Fabrication sequences for thin-film circuits
- Design of resistors
- Design of capacitors
- Conductor films
- Layout of thin-film circuits

Fourth Day P.M.

Thick-Film Circuits
- Introduction
- Qualitative description of the thick-film process
- Conductive inks
- Resistive inks
- Dielectric inks
- Design and layout of thick-film resistors
- Design and layout of thick-film capacitors
- Circuit partitioning
- Substate
- Mounting of chips and other discrete components

Fifth Day A.M.

Assembly Techniques
- Chip bonding
- Wire bonding
- Beam leads
- Tape-carrier packaging
- Inverted chips
- Packages
- Thermal considerations

Fifth Day P.M.

In-Process Measurement and Testing of Integrated Circuits

- Introduction
- Four-point probe measurement of resistivity
- Resistivity and carrier mobility
- Film thickness—interference techniques
- Measurement of junction depth
- Measurement of impurity profiles
- Introducton to testing
- Testing of digital circuits
- Testing memories
- Testing of analog circuits
- Functional testing of a hybrid analog circuit
- Automatic test equipment
- Economics of integrated circuit testing

INSTRUCTOR

Gerald E. Subak-Sharpe earned a Ph.D. from the University of London in 1965 and a D.Sc. from Columbia University in 1969. Since 1968, after industrial experience in Britain and with the Bell Laboratories in the United States, he has been a member of the Department of Electrical Engineering, City University of New York, City College. He has published many papers on circuit theory and electronics and is co-author (with Dr. A. B. Glaser of the Bell Laboratories) of *Integrated Circuit Engineering.* Dr. Subak-Sharpe is a fellow of the Institute of Electrical Engineers, London, and a senior member of IEEE.

TEXT

Integrated Circuit Engineering, by A. B. Glaser and G. E. Subak-Sharpe, Addison-Wesley Publishing Company: Reading, Mass., 1977.

FEE

The fee for the course is $705. This includes lecture notes, text , and supplies. Make checks and purchase orders payable to GWU, Continuing Engineering Education. Participants may delay payment until arrival.

Course No. 696

ENGINEERING OF VERY LARGE SCALE INTEGRATION

June 15-17, 1981

COURSE OBJECTIVE

This course is designed to provide participants with a comprehensive coverage of the engineering of very large scale integrated circuits.

WHO SHOULD ATTEND

Technical managers, engineers, scientists, and others working in the electronics industry who require a better understanding of the engineering of very large scale integrated circuits.

BACKGROUND

Very reliable low-cost VLSI circuits, consisting of very small electronic devices, are performing complex functions at increasingly higher speeds. During the last decade, engineers placed a microprocessor on a chip and will soon place a whole system on a chip. This can be accomplished only with new system architecture and software coupled with design for reliability and testability.

DESCRIPTION

The course begins with a review of integrated circuit technology, both past and present. This is followed by a discussion of the implications of component down-scaling and inherent performance limits for VLSI. Fabrication technologies, particularly NMOS, CMOS, and MESFET, are described, as well as the new optical, x-ray, and electron-beam lithographies. Dry lithographic processing and cold processing techniques are described. The latter part of the course deals with the important topics of computer-aided circuit design (CAD), layout, and testing.

PREREQUISITE

There is no specific prerequisite for this course. However, some knowledge of semiconductors would be helpful.

OUTLINE

First Day

Review and Overview of VLSI

- Component density and chip size projections
- Stage delay — power projections
- Economic and cost predictions
- Computer-aided design (CAD) and layout approaches
- Test problems, reliability, and failure
- Future goals for memories and processors

Down-Scaling and Performance

- Physical limits — laws of nature
- Technological limits — material constants and electrical parameters
- Limits imposed by the physics and chemistry of fabrication
- Component density limits

Fabrication Technologies

- NMOS
- CMOS
- CMOS/SOS

- MESFETS
- GaAs

Second Day

Lithography
- Optical lithography
- Contact and proximity printing
- Optical resists
- High-resolution optical systems
- Electron lithography
- Electron guns and magnetic lenses
- Electron beam lithography
- Electron resists
- Vector scan and patterning schemes
- X-ray lithography
- X-ray sources and systems
- X-ray proximity printing
- X-ray masks and patterning

Processing
- Ion milling
- Plasma etching
- Reactive ion-beam etching
- Cold processing techniques
- Ion implantation
- Low pressure film deposition

Third Day

CAD and Layout
- Pictorial forms for designer-computer interfacing
- Pictures, color, schematics, diagrams, and graphs
- Interactive design techniques
- Designer-controlled computer processing
- Structured design methodologies
- Circuit analysis and simulation
- Symbolic layout
- Layout and logic verification
- System test
- Databases and data management

Testing
- Economics of production testing
- Test time and test cost
- Economics of design verification testing
- Fault models
- Cost of test generation
- Test cost vs. design cost
- Strategy for testing
- Design for testability
- Test point philosophy
- Modularization of logic and layout
- Vector generation
- Test equipment
- Test reduction by means of redundancy and fault-tolerant design

INSTRUCTOR

Gerald E. Subak-Sharpe (See Course No. 574.)

TEXT

Introduction to VLSI Systems by Carver Mead, Professor of Computer Science, California Institute of Technology, and Lynn Conway, Manager, LSI Systems Area, Palo Alto Research Center, Xerox Corporation; Addison-Wesley Publishing Company: Reading, Mass., 1979.

FEE

The fee for the course is $575. This includes lecture notes, text , and supplies. Make checks and purchase orders payable to GWU, Continuing Engineering Education. Participants may delay payment until arrival.

Course No. 677

DESIGN OF DIGITAL CONTROL SYSTEMS

June 22-25, 1981

WHO SHOULD ATTEND

This course is structured for system designers, engineers, scientists, and others who require a knowledge of analysis and design techniques for closed-loop digital control systems.

DESCRIPTION

This course presents the mathematical concepts needed for understanding the operation of both sampled-data control systems and digital control systems. Simple mathematical developments are emphasized to permit those without extensive mathematical backgrounds to understand the material. Also included are computer programs, written in either BASIC or FORTRAN, needed for the analysis and design of digital control systems. Practical aspects of analysis and design are emphasized.

Two case studies of operational systems — one simple and one complex — are discussed. The first is the design of a temperature control system for an environmental plant chamber, using a TI 9900 microprocessor-based digital controller. The second is the design of a lateral control system for the automatic landing of aircraft, using a Sperry-Univac UYK-20 minicomputer as the controller. Both systems were designed using frequency-response techniques, which are emphasized throughout this course.

PREREQUISITE

While there is no prerequisite for this course, some background in linear system analysis, e.g., circuit analysis, would be helpful.

OUTLINE

Difference Equations and z-Transforms
Discrete-time system models, the z-transform, simulation diagrams

Basic Sampling Theory
Sampled-data systems, the ideal sampler, effects of sampling, data reconstruction

Discrete-Time System Models
The pulse transfer function, transfer functions of closed-loop digital control systems

Stability of Discrete-Time Systems
Jury test, root locus, Nyquist criterion, Bode diagrams, frequency response

Digital Controller Design by Frequency-Response Techniques
Bode technique, phase-lead and phase-lag controllers, proportional-plus-integral-plus-derivative (PID) controllers

State Variables for Discrete-Time Systems: an Introduction
State variables for analog systems; state variables for discrete-time systems

Modern Digital Controller Design: an Overview
Observers, Kalman filters; advantages and limitations

Case Studies
Two operational digital control systems using PID controllers

INSTRUCTOR

Charles L. Phillips, Ph.D., is Professor of Electrical Engineering at Auburn University. Dr. Phillips' research interest is automatic control, particularly digital control, on which he is currently writing a textbook. He has performed research and design on the application of digital control theory of large space vehicles, missiles, automatic landing systems for U.S. Navy aircraft, and environmental plant chambers. He has implemented digital controllers based on the Intel 8080 and 8085 microprocessors, and the TI 9900 microprocessor. He has written extensively in the field of digital control.

FEE

The fee for the course is $645. This includes lecture notes and supplies. Make checks and purchase orders payable to GWU, Continuing Engineering Education. Participants may delay payment until arrival.

Course No. 828

COMPUTER COMMUNICATIONS CONCEPTS

June 29-30, 1981

COURSE OBJECTIVE

To provide participants with a brief but comprehensive survey of computer communications concept.

WHO SHOULD ATTEND

Managers and staff personnel responsible for the purchase and management of telecommunications systems, communications system designers and analysts responsible for initial design in automating corporate business procedures, and teleprocessing services sales personnel responsible for sales of computer services and hardware.

DESCRIPTION

This course is structured to cover the fundamentals of automated data communications, using a task-oriented instruction technique to provide an understanding of the terminology and technicalities of computer communications. Upon completion of this course, the participant should be able to apply computer communications concepts, arrange components to form a working system, use correct terminology to describe communications systems, identify incompatibilities within a communication system, predict system performance, and recognize the computer communications requirements in various business situations.

PREREQUISITE

There is no specific prerequisite for this course. However, some knowledge of communications networks would be helpful.

OUTLINE

System Components and Compatibility
- Types, functions, and characteristics of all elements in a data communications system
- Current data terminology and technology (bit, baud, synchronous, asynchronous, duplex, half-duplex, etc.)
- System construction and compatibility

Data Transfer
- Three components of data transfer (connection, transfer medium, and verification)
- Function and rationale for controls and protocol
- Error detection and retransmission techniques (ACK and NAK messages, BCC, etc.)

Effective Data Transfer Rate
- Factors that affect through-put on a two-point data channel (block size, transmission speed, error rate, code structure, etc.)

Data Communications Criteria
- Factors considered in design of data communications systems (volume, function, distribution, etc.)
- Interrelation of system design criteria

System Evaluation
- Examination of an existing communications system and evaluation of three alternatives
- Evaluation of system implications based on changes in through-put, volume, technology, costs, etc.

INSTRUCTOR

Gord Warner has eight years of experience as a telecommunications consultant and has extensive experience in background analysis, system design, and implementation. He has been teaching courses at Bell Canada's Customer Education Center in Toronto. He has also served as a marketing consultant for videotex systems in Canada.

FEE

The fee for this course is $425. This includes lecture notes and supplies. Make checks and purchase orders payable to GWU, Continuing Engineering Education. Participants may delay payment until arrival.

Course No. 796

DIGITAL INTEGRATED CIRCUITS

July 13-17, 1981

COURSE OBJECTIVE

To provide participants with a comprehensive basic survey of the operation and use of digital integrated circuits.

WHO SHOULD ATTEND

Engineers and technical personnel who require an enhanced knowledge of digital integrated circuits, including field servicemen who are required to resolve problems involving logic circuits; field managers who wish to update their knowledge of logic circuitry; and educational personnel who are required to provide instruction concerning computer hardware and peripheral devices.

DESCRIPTION

This course is designed to provide participants with a basic knowledge of the operation and use of digital integrated circuits. The operation of gate-equivalent circuitry for the more basic units will be covered. The different scales of integration (SSI, MSI, and LSI) will be described in terms of gate-equivalent circuitry. Types of packaging and pin allocations used in integrated circuits will be covered as well as the reading and interpretation of logic diagrams. The operation and use of advanced logic units (line drivers, decoders, comparators, etc.), specialized devices (UART, MPU, ALU, etc.), MOS devices (ROM, PROM, EPROM, etc.) and the different types of memories being produced today will be described. Reference material will be provided, covering a variety of related subjects such as logic chip packaging, common logic chips, MOS/LSI monolithic circuit descriptions, 8080 CPU unit diagrams and descriptions, and memory devices.

PREREQUISITE

There is no specific academic prerequisite for this course. However, some knowledge of solid state electronics and digital logic would be helpful.

OUTLINE

Gate-equivalent Circuitry
- Flip-flops
- Basic functions

Scales of Integration
- SSI
- MSI
- LSI

Packaging
Logic Diagram Interpretation
Advanced Units
- Line drivers
- Decoders
- Comparators and other units

Specialized Devices
- UART
- MPU
- ALU and others

MOS Devices
- Read-only memories
- Programmable read-only memories

Memories
- Types of memories in use
- Operation

INSTRUCTOR

Robert J. Cameron is a Senior Analyst for the Computer Training Group of Bell Canada. Working in the area of data communication technology, he participated in the development of the DATAPAC packet switching network in Canada. He has been a lecturer and consultant to private companies and government agencies in the field of data communications.

FEE

The fee for this course is $705. This includes lecture notes and supplies. Make checks and purchase orders payable to GWU, Continuing Engineering Education. Participants may delay payment until arrival.

PLEASE RETURN ENTIRE PANEL

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Name _____ A
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D

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☐ Register me for course no. _____ Date _____ K

Please send information on courses numbered:

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☐ I am not interested in attending these courses but please add my name to your mailing list to receive announcements of future sessions.

Course No.	Title	Date
574	Integrated Circuit Engineering	June 8-12, 1981
696	Engineering of Very Large Scale Integration	June 15-17, 1981
677	Design of Digital Control Systems	June 22-25, 1981
828	Computer Communications Concepts	June 29-30, 1981
796	Digital Integrated Circuits	July 13-17, 1981

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HOUSING AND MEALS

Housing and meals are not provided. However, there is a wide variety of hotels, motels, and restaurants nearby. Since hotel accommodations may be difficult to obtain, reservations should be made as early as possible. If you have difficulty obtaining reservations, we will be happy to assist you.

TIME AND PLACE

Check-in will be at 8:15 a.m. on the first day of each course in the 6th floor lobby of the University's Gelman Library, 2130 H St., N.W. (corner of 22nd and H), Washington, D.C. Classes will meet from 8:30 a.m. to 4:15 p.m. Parking is provided.

REGISTRATION

Tentative or final registration should be made as soon as practicable. Fill out and mail the attached registration form, or apply by letter, telephone, TELEX, or purchase order to Continuing Engineering Education Program, George Washington University, Washington, D.C. 20052, **(202) 676-6106,** the toll free number **(800) 424-9773,** or **TELEX 64374 (International).**

To facilitate registration by telephone, please mention the alphabetical priority code immediately to the right of the registration panel.

CONTINUING EDUCATION UNITS (CEU)

Course participants will receive a Certificate of Completion indicating the number of Continuing Education Units (CEUs) awarded for the course. The CEU is a standard measurement for noncredit continuing education programs. One CEU is given for each 10 contact hours in the classroom.

TEAM DISCOUNTS

Organizations are encouraged to take advantage of fee reductions for multiple registrations for the same course. Discounts of 10% are allowed for three to four registrants, 15% for five to nine registrants, and 20% for ten or more registrants from the same organization.

SPECIAL COURSES

Most of our courses can be presented on an in-house contract basis. New courses can be developed based on the specific training needs of your organization. In either case, the cost per capita is substantially lower than advertised fees. We will be happy to provide you with additional information.

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